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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/491,302	01/25/00	GEISSINGER J	55271USA6A

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EXAMINER	
BROCK II,P	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED:
10/30/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/491,302	GEISSINGER ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sh et with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *5-7 and 20-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413) Paper No(s). _____
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) ☐ Notice of Informal Patent Application (PTO-152)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6 and 8* .	6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II and Species A in Paper No. 9 is acknowledged.

The applicant has determined that claims 5, 6 and 20 do not pertain to the elected species. It should be noted that claim 7 is dependent from claim 7 and will be treated as part of the non-elected species.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 19 recites the limitation "each solder ball pad" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim. This claim will be treated as dependent from claim 18.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Higgins, III (USPAT 5639989, Higgins).

Higgins discloses in figure 3 an electronic package (10). Higgins discloses in figure 3 a conductive trace layer having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads (18 and 21). Higgins discloses in figure 3 a dielectric substrate (24) mounted on the first side of the conductive trace layer. Higgins discloses in figure 3 a capacitor including a first conductive layer (22), a second conductive layer (25) and a layer of dielectric material disposed between the first and the second conductive layers, the first conductive layer mounted adjacent to the second side of the conductive trace layer. Higgins discloses in figure 3 a plurality of interconnect regions extending through the first conductive layer and the dielectric material layer of the capacitor. Higgins discloses in figure 3 an interconnect member connected between each of the conductive layer s of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

6. Claims 1 – 3, 12 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kabumoto et al. (USPAT 5883428, Kabumoto).

Kabumoto discloses in figure 1 an electronic package (4). Kabumoto discloses in figure 1 a conductive trace layer (5) having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads (5a and 5b). Kabumoto discloses in figure 1 a dielectric substrate (1) mounted on the first side of the conductive trace layer. Kabumoto discloses in figure 1 a capacitor including a first conductive layer (10), a second conductive layer (11) and a layer of dielectric material disposed between the first and the second conductive layers, the first conductive layer mounted adjacent to the second side of the conductive trace layer. Kabumoto discloses in figure 1 a plurality of interconnect regions (12a – 12d) extending through the first conductive layer and the dielectric material layer of the capacitor. Kabumoto discloses in figure 1 an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected (12a) to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected (12b) to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

With regard to claim 2, Kabumoto discloses in column 5, lines 23 – 34 wherein the first electrode is maintained at a first reference voltage and wherein the second electrode is maintained at a second reference voltage different from the first reference voltage.

With regard to claim 3, Kabumoto discloses in figure 1 an electrically conductive stiffening member (H) mounted adjacent to the second conductive layer of the capacitor.

With regard to claim 12, Kabumoto discloses in column 6, lines 43 – 47 wherein the dielectric material of the capacitor includes a metal oxide.

With regard to claim 17, Kabumoto discloses in figure 1 wherein the interconnect member is a solder plug.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto as applied to claims 1 and 3 above, and further in view of Dehaine et al. (USPAT 4982311, Dehaine).

Kabumoto disclose in figure 1 a device receiving region extending through the dielectric substrate and the conductive trace layer and further comprises an electronic component (3) mounted in the device receiving region. Kabumoto does not disclose the device receiving region also extends through the capacitor and further comprises the electronic device mounted on the stiffening member. Dehaine discloses in figure 1 a device receiving region extending through a dielectric substrate, a conductive trace layer, a capacitor (18a and 18b) and further comprises an electronic component (12) mounted in the device receiving region on a stiffening member (20). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the receiving region of Dehaine in the device of Kabumoto in order to allow easy refrigeration of the electronic device as stated by Dehaine in column 2, lines 33 – 40.

9. Claims 8 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto as applied to claim 1 above, and further in view of Parker et al. (USPAT 5633785, Parker).

Kabumoto does not disclose the capacitance of the capacitor. Parker discloses in column 7, lines 8 – 12 a capacitor that has a capacitance of from about 5 nF/sq.cm. to about 30 nF/sq.cm. or of at least 30 nF/sq.cm. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the capacitance range of Parker in the device of Kabumoto in order to reduce power consumed by the electronic device as stated by Parker in column 7, lines 14 – 17.

10. Claims 14 – 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto as applied to claim 1 above, and further in view of Fujisawa et al. (USPAT 6184567, Fujisawa).

With regard to claim 14, Kabumoto does not disclose that the dielectric substrate includes a plurality of apertures. Fujisawa teaches in figure 8 wherein a dielectric substrate (12) includes a plurality of apertures, each one of the apertures being positioned adjacent to one of an interconnect regions of a capacitor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the plurality of apertures of Fujisawa in the device of Kabumoto in order to ensure insulation between contact pads of the trace layer.

With regard to claims 15 and 16, Kabumoto does not disclose that the dielectric substrate includes a polymeric film that is a polyimide film. Fujisawa discloses in column 3, line 19 wherein a dielectric substrate includes a polymeric film that is a polyimide film. It would have

been obvious to one of ordinary skill in the art at the time of the present invention to use the polyimide film of Fujisawa in the device of Kabumoto in order to resist metallization while bonding to the electronic device.

With regard to claim 18, Kabumoto does not disclose wherein each interconnect pad is a solder plug. Fujisawa discloses in figure 8 interconnect pad (28 and 32) is a solder ball pad. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the solderball pad of Fujisawa as the interconnect pad in the device of Kabumoto in order to use flip chip bonding for the connection.

With regard to claim 19, With respect to claims 14 and 18 above it further would have been obvious in the method of Kabumoto and Fujisawa that the dielectric substrate has an aperture extending threrethrough adjacent each solderball pad.

11. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto as applied to claim 1 above, and further in view of Brandt et al. (USPAT 6068782, Brandt).

With regard to claim 11, Kabumoto does not disclose a dielectric thickness of from about 5um to about 30 um. Brandt teaches in column 4, lines 35 – 37 a thickness of a dielectric material of a capacitor within the claimed range. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Brandt in the device of Kabumoto in order to have a useful thickness for a dielectric layer of a capacitor in a semiconductor package as stated by Brandt in column 4, lines 35 – 37.

With regard to claim 13, Kabumoto does not disclose a dielectric material made of a non-conductive polymer with high dielectric particles. Brandt discloses in column 4, lines 18 – 41 a dielectric material made of a non-conductive polymer with high dielectric particles of lead zirconium titinate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric material of Brandt in the method of Kabumoto in order to form an efficient embedded capacitor that can be incorporated into layers of a PCB in order to more efficiently and effectively utilize available space.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Furukawa et al. discloses a high dielectric film. Imura et al. discloses a package for a semiconductor device with an embedded capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
October 25, 2001

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